REMARKS

The Examiner's Action mailed on December 23, 2006, has been received and its contents carefully considered. Additionally attached to this Amendment is a Request for Continued Examination (RCE).

In this Amendment, Applicants have amended claims 2, 5-6, 9-10 and 18, canceled claims 3-4, 16-17, 19, 26-32 and 35-36. Claim 5 is the independent claim, and claims 2, 5-6, 9-10, 18 and 20 remain pending in the application. For at least the following reasons, it is submitted that this application is in condition for allowance.

The Examiner has rejected claims 2 and 5 as being anticipated by *Zhang et al.* (USP 6,255,705). It is submitted that these claims are *prima facie* patentably distinguishable over the cited reference for at least the following reasons.

Applicants' amended independent claim 5 is directed to a semiconductor apparatus which includes a silicon substrate having an integrated circuit and a rough or irregular surface due to at least a wiring pattern of the integrated circuit. A planarized region is defined over the rough or irregular surface and a planarized region is disposed over the planarized region. Claim 5 further recites that a semiconductor thin film including a light-emitting element is bonded on the planarized film, so that the semiconductor thin film is disposed above the integrated circuit and the planarized film electrically connects the light-emitting elements to the integrated circuit. This invention has the advantages discussed in

Applicants' specification, and is neither disclosed nor suggested by the cited reference.

Zhang et al. is directed to a device having both active matrix display circuits and peripheral circuits on the same substrate. The Examiner's Action has relied on the embodiment shown in Figures 1e and 3b in establishing his anticipation rejection. In particular, the Examiner's Action has equated the active layers 125, 126 and 127 as being the semiconductor thin film as recited in claim 5. However, these features form a component of the TFTs 151, 152 and 153, and, in fact, form a lowermost portion of the TFTs 151, 152 and 153. Thus, the active layers 125, 126 and 127 are not disposed above the TFTs 151, 152 and 153, whereas, in amended claim 5, the semiconductor thin film is disposed above the integrated circuit.

The Examiner's Action has equated the underlying film 102 disclosed by *Zhang et al.* as being the planarized film recited in claim 5. The underlying film 102 as disclosed by *Zhang et al.* is disposed on the insulating surface of the substrate 101 and is formed of silicon oxide (see *Zhang et al.* Col. 11, Lines 66-67). However, the underlying film 102 does not have anything to do with the electrical connection of one element of the device to another element of the device, whereas, in claim 5, the planarized film electrically connects the light-emitting elements to the integrated circuit. Accordingly, the planarized film recited in amended claim 5 is not disclosed or suggested by *Zhang et al.*

Moreover, the silicon substrate recited in amended claim 5 is not disclosed or suggested by *Zhang et al.* The substrate 101 formed under the underlying film 102, as disclosed by *Zhang et al.,* does not have any rough or irregular surface (see *Zhang et al.* Figure 1E). In contrast, the silicon substrate has a rough or irregular surface due to at least the wiring pattern of the integrated circuit formed thereon.

As such, it is submitted that Applicants' independent claim 5, and the claims dependent therefrom, have not been anticipated by the cited reference. It is thus requested that these rejections be withdrawn and that these claims be allowed.

The Examiner's Action has rejected claim 3, 6 and 18 as being obvious over *Zhang et al.* in view of *Walker et al.* (USP 6,841,813). Because all features in claim 3 are added to amended claim 5, Applicant will treat this rejection as pertaining to claim 5. However, it is submitted that independent claim 5 and claims 6 and 18 that depend therefrom are *prima facie* patentably distinguishable over cited combination of references for at least the following reasons.

Initially, it is noted that *Walker et al.* do not overcome the above-noted deficiencies of *Zhang et al.* In particular, *Walker et al.* disclose a three-dimensional semiconductor apparatus that includes a plurality of device levels 2 separated by interlevel insulating layers. The Examiner's Action has equated the interlevel insulating layer 3B disclosed by *Walker et al.* as being the planarized film recited in claim 5. However, the interlevel insulating layer 3B comprises one

or more of silicon oxide, silicon oxynitride, silicon nitride, spin-on glass, BPSG, PSG, BSG or any other insulating layers (see *Walker et al.* Col. 6, Lines 46-50). The interlevel insulating layer 3B disclosed by *Walker et al.* insulates the first device level 2A from the second device level 2B (see Col. 6, Lines 53-55, Figures 3 and 4D). On the contrary, the planarized film as recited in claim 5 electrically connects the light-emitting elements to the integrated circuit. Since, the reference does not disclose or suggest the planarized film semiconductor thin as recited in claim 5, independent claim 5 and dependent claims 6 and 18 are submitted to be *prima facie* patentably distinguishable over the cited combination of references.

The Examiner has also rejected claim 20 as being obvious over *Zhang et al.* in view of *Hayashi et al.* (JP 09045930). Because *Hayashi et al.* do not overcome the above noted deficiencies of *Zhang et al.*, it is submitted that claims 20 is *prima facie* patentably distinguishable over the cited references for at least the same reasons as independent claim 5, from which this claim depend, as well as for the additional features recited therein. It is requested that the claim be allowed and that this rejection be withdrawn.

The Examiner's Action has also rejected independent claim 5 and dependent claims 9 and 10 as being obvious over *Zhang* (US 2003/0067043) in view of *Muto et al.* (JP 61102767). It is submitted that these claims are *prima facie* patentably distinguishable over the cited references for at least the following reasons.

The Examiner's Action has equated the substrate circuit 0s disclosed by *Zhang* as being the silicon substrate as recited in claim 5. However, the substrate circuit 0s does not have any rough or irregular surface (see *Zhang* Figures 1A and 2A).

The Examiner's Action has also equated the config-dielectric 23 disclosed by *Zhang* as being the planarized film recited in claim 5. However, the config-dielectric 23 isolates the word line 20a from the bit line 30c (see Paragraph [0101] and Figure 9A). In contrast, the planarized film recited in claim 5 electrically connects the light-emitting elements to the integrated circuit. Accordingly, the planarized film recited in claim 5 is not disclosed or suggested by *Zhang.*

In addition, *Zhang* does not disclose or suggest a semiconductor thin film including a light-emitting element as recited in amended claim 5. More specifically, a natural P+/N-/N+ diode formed by word line 20a disclosed by *Zhang* is not equivalent to the light-emitting element recited in claim 5.

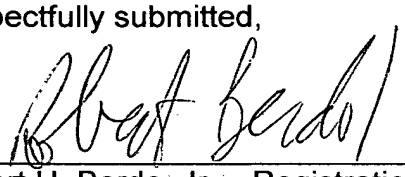
Muto et al. do not overcome the above noted deficiencies of *Zhang.* As such, it is submitted that Applicants' independent claim 5 and the claims dependent therefrom, are *prima facie* patentably distinguishable over the cited combination of references. It is requested that these claims be allowed and that these rejections be withdrawn.

It is submitted that this application is now in condition for allowance. Such action and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of the application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Should any fee be required, the Commissionaire is hereby authorized to charge the fee to our deposit account No. 18-0002, and notify us accordingly.

Respectfully submitted,



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Date

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